CLAIMS

1. An anti-jitter circuit for reducing time jitter in an input pulse train comprising,

an integrator charge storage means,

charging means for deriving from the input pulse train at least one charge packet during each cycle of the input pulse train and for supplying the charge packets to the integrator charge storage means, and

discharging means for continuously discharging the integrator charge storage means,

the charging means and the discharging means being operative to create on the integrator charge storage means a time varying voltage waveform having a mean d.c. voltage level, and

means for comparing said time varying voltage waveform with said mean d.c. voltage level and deriving an output pulse train as a result of the comparison.

2. An anti-jitter circuit as claimed in claim 1 wherein said discharging means comprises a discharge device having a control input and means defining a negative feedback path between the control input and an output of the integrator charge storage means whereby to maintain said mean d.c. voltage level substantially constant.

3. An anti-jitter circuit as claimed in claim 2 wherein said discharge device is a current source or a current sink.

4. An anti-jitter circuit as claimed in claim 3 wherein said discharge device is a transistor.

5. An anti-jitter circuit is claimed in any one of the claims 2 to 4 wherein said means defining a negative feedback path comprises a low pass filter.

6. An anti-jitter circuit as claimed in claim 5 wherein the negative feedback path is formed by the combination of a resistor and a capacitor.

7. An anti-jitter circuit as claimed in any one of claims 2 to 6 wherein said mean d.c. voltage level is generated at an output of said negative feedback path and said means for comparing comprises a comparator having a first input coupled to the integrator charge storage means and a second input coupled to said output of the negative feedback path.

8. An anti-jitter circuit is claimed in any one of the claims 2 to 7 including a monostable circuit connected to the output of said means for comparing.

9. An anti-jitter circuit as claimed in claim 8 wherein said mean d.c. voltage level is used to control the pulse length of pulses output by the monostable circuit.

10. An anti-jitter circuit as claimed in claim 9 wherein the monostable circuit is a

current-controlled monostable circuit and has a control input coupled to the output of said negative feedback path by a current mirror matched to said discharge device.

11. An anti-jitter circuit as claimed in claim 10 wherein said discharge device and said current mirror are matched transistors.

12. An anti-jitter circuit as claimed in any one of claims 8 to 11 wherein said monostable circuit is triggered whenever a discharge part of the time-varying voltage waveform crosses the mean d.c. level.

13. An anti-jitter circuit as claimed in any one of claims 1 to 12 including frequency doubling means comprising a first said charging means and a second said charging means for deriving charge packets respectively from the rising and falling edges of the input pulse train.

14. An anti-jitter circuit as claimed in any one of claims 1 to 13 including means for maintaining the charge value of the charge packets substantially constant.

15. An anti-jitter circuit as claimed in claim 14 wherein said means for maintaining comprises a further transistor coupled between said charging means and said integrator charge storage means.

25 16. An anti-jitter circuit as claimed in claim 15 wherein said further transistor is arranged to operate in grounded base mode.

26 17. An anti-jitter circuit as claimed in claim 16 including averaging means connected to the base of the further transistor.

27 18. An anti-jitter circuit as claimed in claim 15 wherein said discharging means includes a first field effect transistor operative as a discharge device and said further transistor is a second field effective transistor, and the gate of the first field effect transistor is connected to the gate of the second field effect transistor.

Sub A-4 19. An anti-jitter circuit as claimed in any one of claims 2 to 6 wherein said means for comparing comprises inverted gate means having an input coupled to the integrator charge storage means and an output, and including means defining a further negative feedback path between said output of said inverted gate means and said discharging means whereby to establish said mean d.c voltage level as a switching level of said inverted gate means.

Sub D1 C 12 20. An anti-jitter circuit as claimed in claim 19 wherein said further negative feedback path is connected between said output of said inverted gate means and said control input of said discharging device.

Subb A5

21. An anti-jitter circuit as claimed in claim 19 or claim 20 wherein said further negative feedback path comprises a low pass filter.

Sub D'

16 15 further

~~22~~. An anti-jitter circuit as claimed in claim ~~21~~ wherein said low pass filter comprises the combination of a resistor and a capacitor.

Subb A-6

23. An anti-jitter circuit as claimed in any one of claims 2 to 6 wherein said means for comparing comprises inverted gate means having an input coupled to the integrator charge storage means and an output, and including a voltage source coupled to the discharging means whereby to establish said mean d.c voltage level as a switching level of said inverted gate means.

Sub D'

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~~24~~. An anti-jitter circuit as claimed in claim ~~23~~ wherein said voltage source is connected between said output of said inverted gate means and said control input of said ~~discharging~~ discharge device.

Subb A-7

25. An anti-jitter circuit as claimed in any one of claims 2 to 24 including means providing a low impedance path between the input and the output of the negative feedback path.

Sub D'

20 19

~~26~~. An anti-jitter circuit as claimed in claim ~~25~~ wherein said low impedance path is formed by diodes connected back-to-back.

27. An anti-jitter circuit as claimed in any one of the claims 1 to 26 wherein the or each said charging means is a charge pump.

28. An anti-jitter circuit substantially as herein described with reference to Figures 2 to 10 of the accompanying drawings.